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VOLPE AND KOENIG, P.C.	LEE, CHRISTOPHER E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/699,145	KAEWELL ET AL.
	Examiner	Art Unit
	Christopher E. Lee	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _02 January 2004_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-23_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _10_.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1.   Receipt is acknowledged of the Amendment filed on 2nd of January 2004. Claim 15 has been

amended; no claim has been canceled; and no claim has been newly added since the last Office Action

was mailed on 3rd of October 2003. Currently, claims 1-23 are pending in this application.

Claim Rejections - 35 USC § 103

2.   The text of those sections of Title 35, U.S. Code not included in this action can be found in a

prior Office action.

3.   Claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Koenig et al. [US 6,101,198 A ; hereinafter Koenig] in view of Applicant Admitted

Prior Art [hereinafter AAPA].

Referring to claim 1, Koenig discloses a modem interface (i.e., processor based voice and data

TSI system 20 of Fig. 4) for transferring data (See col. 1, lines 4-10) between a first high data rate

interface (i.e., T-1 48 of Fig. 4) and a second high data rate interface (i.e., T-1 50 of Fig. 4), said modem

interface comprising: a plurality of parallel data highways (i.e., PCM highways 36, 38, 40, 42, 52, 54, 56,

58 and V.35 high-speed serial port 64 in Fig. 4, in parallel) having frames with time slots for transferring

data (See col. 8, lines 9-23 and col. 9, lines 38-62), said plurality of data highways outputting (e.g.,

framing by Framer 60 of Fig. 4) data to said first and second high data rate interfaces (e.g., T-1 48 and T-

1 50, respectively, in Fig. 4) in selected time slots (See col. 11, lines 43-50), each data highway being at

least partially dedicated to a separate function (See col. 7, lines 14-56 and 64-67; i.e., wherein in fact that

(1) two PCM highways (i.e., 36 and 38 in Fig. 4) come from a pair of conventional T-1 lines via

conventional framers, which provide signal conditioning and strip the frame bit, (2) the other two PCM

highways (i.e., 40 and 42 in Fig. 4) are created by FX cards, which convert a plurality of analog phone

lines to digital and multiplex these digital representations, among other things, (3) two of PCM highways

(i.e., 52 and 54 in Fig. 4) are connected to the framers, (4) the other two PCM highways (i.e., 56 and 58 in Fig. 4) connect to FX cards, which demultiplex the signals and convert to analog phone lines, and (5) the built-in V.35 DCE data port is dedicated to Internet, video, or WAN implies each data highway being at least partially dedicated to a separate function); at least one of said data highways (e.g., PCM highway 36

5   in Fig. 4) receiving data from said first high data rate interface (i.e., T-1 48 of Fig. 4); at least one of said data highways (e.g., PCM highway 38 in Fig. 4) having an input (e.g., Framer 44 of Fig. 4) configured to receive data from said second high data rate interface (i.e., T-1 50 of Fig. 4) in selected time slots (See col. 11, lines 43-50); and a first processor (i.e., DSP (Engine) 24 of Fig. 4) for controlling data transfer between said plurality of data highways (See col. 11, lines 58-65) and sending data using a sub-plurality

10   of said data highways (i.e., sending analog data using a sub-plurality of PCM highways 56, 58, and sending digital data using another sub-plurality of PCM highways 52, 54); and a second processor (i.e.,   . DSP (Host) 22 of Fig. 4) sending data (e.g., data for Internet, video, or WAN applications; See col. 7, lines 65-67) using a single one of said data highways (i.e., V.35 high-speed serial port 64 in Fig. 4). Koenig does not expressly teach said second high data rate interface is a wireless interface.

15   AAPA discloses a modem interface (See MODEM interface 34 of Fig. 1 and page 1, line 8 through page 2, line 10), wherein said modem interface for transferring data (See page 1, lines 8-10) between an user terminal 46 (Fig. 1) and a second high data rate interface, which is a wireless interface (i.e., wireless air interface 38 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

20   made to have substituted said wireless interface, as disclosed by AAPA, for said second high data rate interface, as disclosed by Koenig, for the advantage of transferring data between wired components of the network and a wireless communication network (See AAPA, page 1, lines 8-13).

    Referring to claim 8, Koenig, as modified by AAPA, teaches said frames have time slots (See the above prior claim 1 rejection), but does not expressly teach said frames have sixteen time slots.

However, the claim recites said sixteen time slots without any patentable advantage in the specification (See claim 8 and Application, page 4, line 17). In other words, the Applicant states a preferred frame would have sixteen (16) time slots, which means said specific number of time slots (16) in a frame is chosen among any number of time slots per frame as a preference of one of ordinary skill in the art.

5   Therefore, the limitation of said sixteen time slots in the claim is not patentably significant since it at most relates to the number of time slots in a frame under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

         Referring to claim 9, Koenig discloses a method for transferring data (See col. 1, lines 4-10) between a first high data rate interface (i.e., T-1 48 of Fig. 4) and a second high data rate interface (i.e., T-

10   1 50 of Fig. 4), said method comprising: a modem interface (i.e., processor based voice and data TSI system 20 of Fig. 4) provides a plurality of parallel data highways (i.e., PCM highways 36, 38, 40, 42, 52, 54, 56, 58 and V.35 high-speed serial port 64 in Fig. 4, in parallel) having frames with time slots for transferring data (See col. 8, lines 9-23 and col. 9, lines 38-62), each data highway being at least partially dedicated to a separate function (See col. 7, lines 14-56 and 64-67; i.e., wherein in fact that (1) two PCM

15   highways (i.e., 36 and 38 in Fig. 4) come from a pair of conventional T-1 lines via conventional framers, which provide signal conditioning and strip the frame bit, (2) the other two PCM highways (i.e., 40 and 42 in Fig. 4) are created by FX cards, which convert a plurality of analog phone lines to digital and multiplex these digital representations, among other things, (3) two of PCM highways (i.e., 52 and 54 in Fig. 4) are connected to the framers, (4) the other two PCM highways (i.e., 56 and 58 in Fig. 4) connect to

20   FX cards, which demultiplex the signals and convert to analog phone lines, and (5) the built-in V.35 DCE data port is dedicated to Internet, video, or WAN implies each data highway being at least partially dedicated to a separate function); inputting data (e.g., via Framer 44 of Fig. 4) to said data highways (e.g., PCM highways 36 and 38 in Fig. 4) from said first and second high data rate interfaces (i.e., T-1 48 and T-1 50 in Fig. 4) in selected time slots (See col. 11, lines 43-50); controlling data transfer between said

plurality of highways (See col. 11, lines 58-65); and outputting data (e.g., via Framer 60 of Fig. 4) to said

first and second high data rate interfaces (i.e., T-1 48 and T-1 50 in Fig. 4) in selected time slots (See col.

11, lines 43-50); and wherein one of said plurality of data highways (e.g., PCM highway 36 in Fig. 4)

only receives data from said first high data rate interface (i.e., T-1 48 of Fig. 4) and a first processor (i.e.,

5   DSP (Engine) 24 of Fig. 4) for sending data using a sub-plurality of said data highways (i.e., sending

analog data using a sub-plurality of PCM highways 56, 58, and sending digital data using another sub-

plurality of PCM highways 52, 54) and a second processor (i.e., DSP (Host) 22 of Fig. 4) sending data

(e.g., data for Internet, video, or WAN applications; See col. 7, lines 65-67) using a single one of said data

highways (i.e., V.35 high-speed serial port 64 in Fig. 4).

10   Koenig does not expressly teach said second high data rate interface is a wireless interface.

AAPA discloses a modem interface (See MODEM interface 34 of Fig. 1 and page 1, line 8 through page

2, line 10), wherein said modem interface for transferring data (See page 1, lines 8-10) between an user

terminal 46 (Fig. 1) and a second high data rate interface, which is a wireless interface (i.e., wireless air

interface 38 of Fig. 1).

15   Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have substituted said wireless interface, as disclosed by AAPA, for said second high data rate

interface, as disclosed by Koenig, for the advantage of transferring data between wired components of the

network and a wireless communication network (See AAPA, page 1, lines 8-13).

   Referring to claims 4 and 12, Koenig teaches said plurality of parallel data highways include

20   three parallel data highways (i.e., N number of parallel data highways; See col. 9, lines 42-51).

   Referring to claims 5 and 13, Koenig, as modified by AAPA, does not teach said each of said

three parallel data highways has a 2 Mb/s data rate, but Koenig teaches each of said N parallel data

highways has a 1.544 Mb/s (See Koenig , col. 9, lines 42-51).

However, the claim recites said 2 Mb/s data rate without any patentable advantage in the specification

(See claim 5 and Application, page 4, lines 18-19). In other words, the Applicant states each data highway

has an associated maximum data rate, such as 2 Mb/s (See Application, page 4, lines 18-19) for the

combined data rate becomes 3 times faster data rate than a single data highway data rate (See Application,

5   page 4, lines 19-21), which means said specific 2 Mb/s data rate is chosen among any data rate of a

specific type of data highway for said modem interface (See Application, page 4, lines 21-23). Therefore,

the limitation of said 2 Mb/s data rate in the claim is not patentably significant since it at most relates to

the data rate of a specific data highway for the data rate matters under consideration which is not

ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

10   *Referring to claim 15,* Koenig discloses a radio network terminal (RNT; i.e., processor based

voice and data TSI system 20 of Fig. 4) for transferring data (See col. 1, lines 4-10) between a first high

data rate interface (i.e., T-1 48 of Fig. 4) and a second high data rate interface (i.e., T-1 50 of Fig. 4), said

RNT comprising: an input and an output for transferring data over said first high data rate interface (See

T-1 50 and Framers 44 & 60 in Fig. 4); a plurality of parallel data highways (i.e., PCM highways 36, 38,

15   40, 42, 52, 54, 56, 58 and V.35 high-speed serial port 64 in Fig. 4, in parallel) having frames with time

slots for transferring data (See col. 8, lines 9-23 and col. 9, lines 38-62), said plurality of data highways

outputting (e.g., framing by Framer 60 of Fig. 4) data to said first and second high data rate interfaces

(e.g., T-1 48 and T-1 50, respectively, in Fig. 4) in selected time slots (See col. 11, lines 43-50), each data

highway being at least partially dedicated to a separate function (See col. 7, lines 14-56 and 64-67; i.e.,

20   wherein in fact that (1) two PCM highways (i.e., 36 and 38 in Fig. 4) come from a pair of conventional T-

1 lines via conventional framers, which provide signal conditioning and strip the frame bit, (2) the other

two PCM highways (i.e., 40 and 42 in Fig. 4) are created by FX cards, which convert a plurality of analog

phone lines to digital and multiplex these digital representations, among other things, (3) two of PCM

highways (i.e., 52 and 54 in Fig. 4) are connected to the framers, (4) the other two PCM highways (i.e.,

56 and 58 in Fig. 4) connect to FX cards, which demultiplex the signals and convert to analog phone

lines, and (5) the built-in V.35 DCE data port is dedicated to Internet, video, or WAN implies each data

highway being at least partially dedicated to a separate function); at least one of said data highways (e.g.,

PCM highway 36 in Fig. 4) only receiving data from said first high data rate interface (i.e., T-1 48 of Fig.

5   4); at least one of said data highways (e.g., PCM highway 38 in Fig. 4) having an input (e.g., Framer 44

of Fig. 4) configured to receive data from said second high data rate interface (i.e., T-1 50 of Fig. 4) in

selected time slots (See col. 11, lines 43-50); and a first processor (i.e., DSP (Engine) 24 of Fig. 4) for

controlling data transfer between said plurality of highways (See col. 11, lines 58-65) and sending data

using a sub-plurality of said data highways (i.e., sending analog data using a sub-plurality of PCM

10   highways 56, 58, and sending digital data using another sub-plurality of PCM highways 52, 54); and a

second processor (i.e., DSP (Host) 22 of Fig. 4) sending data (e.g., data for Internet, video, or WAN

applications; See col. 7, lines 65-67) using a single one of said data highways (i.e., V.35 high-speed serial

port 64 in Fig. 4).

Koenig does not expressly teach said second high data rate interface is a wireless interface; and a receiver

15   and a transmitter for transferring data over said wireless interface.

AAPA discloses a modem (MODEM 28 of Fig. 1), wherein said modem for transferring data (See page 1,

lines 8-10) between an user terminal 46 (Fig. 1) and a second high data rate interface, which is a wireless

interface (i.e., wireless air interface 38 of Fig. 1); and a receiver (i.e., receive circuitry 32 of Fig. 1) and a

transmitter (i.e., transmit circuitry 36 of Fig. 1) for transferring data over said wireless interface (See page

20   1, lines 17-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have included said transmitter and said receiver, as disclosed by AAPA, in said radio network

terminal, as disclosed by Koenig, for the advantage of transferring data between wired components of the

network and a wireless communication network (See AAPA, page 1, lines 8-13).

Referring to claim 18, Koenig, as modified by AAPA, teaches said frames have time slots (See the above prior claim 15 rejection), but does not expressly teach said frames have sixteen time slots. However, the claim recites said sixteen time slots without any patentable advantage in the specification (See claim 8 and Application, page 4, line 17). In other words, the Applicant states a preferred frame

5   would have sixteen (16) time slots, which means said specific number of time slots (16) in a frame is chosen among any number of time slots per frame as a preference of one of ordinary skill in the art. Therefore, the limitation of said sixteen time slots in the claim is not patentably significant since it at most relates to the number of time slots in a frame under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

10   *Referring to claim 19,* Koenig teaches said plurality of parallel data highways include three parallel data highways (i.e., N number of parallel data highways; See col. 9, lines 42-51).

4.   Claims 2, 3, 10, 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig [US 6,101,198 A] in view of AAPA as applied to claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 above, and further in view of Mergard et al. [US 6,415,348 B1; hereinafter Mergard].

15   *Referring to claims 2, 3, 10 and 11,* Koenig, as modified by AAPA, discloses all the limitations of the claims 2, 3, 10 and 11, respectively, except that does not teach said first high data rate interface is an IOM-2 highway or a PCM highway.

Mergard teaches a High-Level Data Link Controller (viz., HDLC controller), wherein Channels of HDLC controller can be coupled to a first high data rate interface (i.e., means for communicating) is an IOM-2

20   highway or a PCM highway (See col. 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said HDLC controller, as disclosed by Mergard, in said modem interface, as disclosed by Koenig, as modified by AAPA, for the advantage of providing a broad range of communications applications (See Mergard, col. 1, lines 25-27).

Referring to claim 20, Koenig, as modified by AAPA, discloses all the limitations of the claim

20, except that does not teach said first high data rate interface is an IOM-2 highway.

Mergard teaches a High-Level Data Link Controller (viz., HDLC controller), wherein Channels of HDLC

controller can be coupled to a first high data rate interface (i.e., means for communicating) is an IOM-2

5   highway (See col. 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have included said HDLC controller, as disclosed by Mergard, in said radio network terminal, as

disclosed by Koenig, as modified by AAPA, for the advantage of providing a broad range of

communications applications (See Mergard, col. 1, lines 25-27).

10   5.   Claims 6, 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig [US

6,101,198 A] in view of AAPA as applied to claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 above, and further

in view of Beyda et al. [US 6,058,111 A; hereinafter Beyda].

Referring to claim 6, Koenig, as modified by AAPA, discloses all the limitations of the claim 6

except that does not teach a plurality of read and write devices, each write device fixedly writing to one of

15   said plurality of data highways and each read device reading data from any of said plurality of data

highways.

Beyda discloses a network (5000 of Fig. 3) in a system for providing a droppable switched circuit,

wherein a plurality of time slot interchangers (i.e., TSIs in Fig.5) comprise: a plurality of read and write

devices (i.e., a plurality of TSI input circuits 5200 and TSI output circuits 5600 in Fig. 5), each write

20   device (i.e., TSI output circuit) fixedly writing to one of a plurality of data highways (i.e., fixedly

outputting to a group of port controllers among a plurality of port controllers 4000-0 through 4000-31in

Fig. 1) and each read device (i.e., TSI input circuit) reading (i.e., inputting) data from any of said plurality

of data highways (i.e., inputting from any of port controllers among a plurality of port controllers 4000-0

through 4000-31in Fig. 1). Refer to col. 6, lines 22-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have combined said time slot interchanges (i.e., TSIs), as disclosed by Beyda, in said processor in

said modem interface, as disclosed by Koenig, as modified by AAPA, for the advantage of being required

to transmit only $1/N^{th}$ (e.g., $1/8^{th}$) of received data (i.e., received digital words), where N is a number of

5   TSI units (e.g., TSI units) during a given frame (See Beyda, col. 6, lines 27-32).

Referring to claim 7, Koenig, as modified by AAPA and Beyda, teaches said processor (i.e., TSI

control circuit 5400 of Fig. 5; Beyda) controls each read device (i.e., TSI input circuit; Beyda) so that

each read device reads from a selected one of said data highways (i.e., so that input TSI input circuits'

data from a selected one of said data highways via SRC ADRS 5487 of Fig. 5; See Beyda, col. 7, lines

10   35-41).

Referring to claim 14, Koenig, as modified by AAPA, discloses all the limitations of the claim 14

except that does not teach said the step of controlling includes using a plurality of read and write devices,

each write device fixedly writes to one of said plurality of data highways and each read device is capable

of reading data from any of said plurality of data highways.

15   Beyda discloses a network (5000 of Fig. 3) in a system for providing a droppable switched circuit,

wherein a step of controlling (See Fig. 3 and 5) includes using a plurality of time slot interchangers (i.e.,

TSIs in Fig.5) comprising a plurality of read and write devices (i.e., a plurality of TSI input circuits 5200

and TSI output circuits 5600 in Fig. 5), each write device (i.e., TSI output circuit) fixedly writes to one of

a plurality of data highways (i.e., fixedly outputs to a group of port controllers among a plurality of port

20   controllers 4000-0 through 4000-31in Fig. 1) and each read device (i.e., TSI input circuit) is capable of

reading (i.e., inputting) data from any of said plurality of data highways (i.e., inputting from any of port

controllers among a plurality of port controllers 4000-0 through 4000-31in Fig. 1). Refer to col. 6, lines

22-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have combined said time slot interchanges (i.e., TSIs), as disclosed by Beyda, in said means for

transferring data, as disclosed by Koenig, as modified by AAPA, for the advantage of being required to

transmit only $1/N^{th}$ (e.g., $1/8^{th}$) of received data (i.e., received digital words), where N is a number of TSI

5   units (e.g., TSI units) during a given frame (See Beyda, col. 6, lines 27-32).

6.   Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig [US 6,101,198 A]

in view of AAPA as applied to claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 above, and further in view of

Rouphael et al. [US 6,301,291 B1; hereinafter Rouphael].

        Referring to claim 16, Koenig, as modified by AAPA, discloses all the limitations of the claim 16

10   except that does not teach said receiver and said transmitter transfer data using QPSK modulation in

CDMA format.

Rouphael discloses a wireless communication systems, wherein a receiver (i.e., Receiver 20 of Fig. 1A)

and a transmitter (i.e., Transmitter 10 of Fig. 1A) transfer data using QPSK modulation in CDMA format

(See Fig. 1 and col. 2, lines 18-42 and col. 3, line 38 through col. 4, line 8).

15   Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have applied said QPSK modulation in CDMA format, as disclosed by Rouphael, to said receiver

and transmitter, as disclosed by Koenig, as modified by AAPA, so as to modulate/demodulate using

QSPK in CDMA format with the advantage of improving data reception (See Rouphael, col. 2, lines 7-

13).

20   7.   Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig [US 6,101,198 A]

in view of AAPA as applied to claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 above, and further in view of

Cannella et al. [US 5,063,592; hereinafter Cannella].

Referring to claim 17, Koenig, as modified by AAPA, discloses all the limitations of the claim 17

except that does not teach said RNT is operatively coupled to an ISDN terminal via said first high data

rate interface.

Cannella discloses a foreign exchange 110 (Fig. 1), wherein an RNT (i.e., switch 112 of Fig. 1) is

5   operatively coupled to an ISDN terminal (i.e., ISDN set 120 of Fig. 1) via a first high data rate interface

(i.e., carrier T-1 line 130 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have coupled said ISDN terminal with its ISDN interface, as disclosed by Cannella, to said radio

network terminal via said first high data rate interface, as disclosed by Koenig, as modified by AAPA, for

10   the advantages of providing both local (i.e., communication among ISDN terminals via ISDN interface,

locally) and said wireless communication service (i.e., foreign exchange services) by said single first high

data rate interface (i.e., single subscriber line). Refer to Cannella, col. 2, lines 29-31.

8.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pillan et al. [US

5,483,556 A; hereinafter Pillan] in view of Shimizu [US 5,381,422 A] and AAPA.

15   *Referring to claim 21,* Pillan discloses a method for data compression/decompression for a HDLC

type frame (See col. 1, lines 8-9 and col. 2, lines 24-34), comprising: producing data (i.e., deriving a first

reduced data frame) having a first high-level data link controlling (HDLC) encoding (See col. 2, lines 55-

57) at a first station (i.e., EMISSION side in Fig. 4) for transfer over a wireless interface (i.e.,

transmission network 3 of Fig. 2); compressing said first HDLC encoded data (i.e., said first reduced data

20   frame) into a second HDLC format (i.e., a first compressed reduced data frame) at said first station (i.e.,

EMISSION side); transmitting said compressed said first HDLC encoded data (i.e., said compressed

reduced data frame) over said wireless interface (See col. 2, lines 61-65); receiving (i.e., restoring) said

compressed said first HDLC encoded data at a second station (i.e., RECEPTION side in Fig. 4; See col.

2, line 65 through col. 3, line 2); and removing (i.e., decompressing) said HDLC compressing (i.e., said

first reduced data frame) to recover said first HDLC encoded data (i.e., an original first data frame; See

col. 3, lines 3-8) at said second station.

Pillan does not expressly teach encoding said first HDLC encoded data into a second HDLC format at

said first station such that said produced data is double HDLC encoded; transmitting said double HDLC

5   encoded data; receiving said double HDLC encoded data at said second station; and removing said second

HDLC encoding to recover said first HDLC encoded data at said second station.

Shimizu discloses a device for correcting code error (See Abstract and col. 1, lines 9-13), wherein said

device performs a step of encoding a first HDLC encoded data (i.e., DPCM data train converted by block

32 from information signal of input terminal 30 in Fig. 2A) into a second HDLC format (i.e., encoded by

10   block 12 for error correction encoding in Fig. 2A) at a first station (i.e., recording system in a data

transmitting system in Fig. 2A) such that a produced data is double HDLC encoded (See col. 2, lines 59-

62); transmitting said double HDLC encoded data (See col. 3, lines 27-31); receiving said double HDLC

encoded data at a second station (i.e., reproducing system in a data transmitting system in Fig. 2B); and

removing said second HDLC encoding to recover said first HDLC encoded data at said second station

15   (See col. 3, lines 35-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have included said double encoding/decoding scheme, as disclosed by Shimizu, in said method

of communicating data, as disclosed by Pillan, for the advantage of providing a code error correcting

feature in which a high processing speed (See Shimizu, col. 1, line 67 through col. 2, line 3).

20   Pillan, as modified by Shimizu, does not expressly teach said method of communicating data over said

wireless interface of a wireless communication network having said first station and said second station.

AAPA teaches a method of communicating data (See Background and Fig. 1) over a wireless interface

(i.e., wireless air interface 38 of Fig. 1) of a wireless communication network (Fig. 1) having a first

station and a second station (i.e., Radio Network Terminal 40 and Radio Carrier Station 26 in Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have applied said method of communicating data, as disclosed by Pillan, as modified by Shimizu,

to said data communication of said wireless communication network, as disclosed by AAPA, for the

advantage of transferring data between wired components of the network and a wireless communication

5   network (See AAPA, page 1, lines 8-13) for complying with a recommendation of reduced transmission

line occupancy (See Pillan, col. 1, lines 12-21).

9.   Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pillan [US

5,483,556 A] in view of Shimizu [US 5,381,422 A] and AAPA as applied to claim 21 above, and further

in view of Mergard [US 6,415,348 B1].

10   *Referring to claim 22,* Pillan, as modified by Shimizu and AAPA, discloses all the limitations of

the claim 22 including said first communication station is a radio network terminal (i.e., Radio Network

Terminal 40 of Fig. 1; AAPA) and said second station is a radio carrier station (i.e., Radio Carrier Station

26 of Fig. 1; AAPA) except that does not teach prior to producing said first HDLC encoded data,

receiving said first HDLC encoded data from an IOM-2 highway.

15   Mergard teaches a High-Level Data Link Controller (viz., HDLC controller), wherein Channels of HDLC

controller can be coupled to a radio network terminal (i.e., Radio Network Terminal) is an IOM-2

highway (See col. 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have included said HDLC controller, as disclosed by Mergard, in said RNT, as disclosed by

20   Pillan, as modified by Shimizu and AAPA, for the advantage of providing a broad range of

communications applications (See Mergard, col. 1, lines 25-27).

Pillan, as modified by Shimizu, AAPA and Mergard, teaches prior to producing said first HDLC encoded

data, receiving said first HDLC encoded data from said IOM-2 highway.

Referring to claim 23, Pillan, as modified by Shimizu and AAPA, discloses all the limitations of the claim 23 including said first station is a radio carrier station (i.e., Radio Carrier Station 26 of Fig. 1; AAPA) and said second station is a radio network terminal (i.e., Radio Network Terminal 40 of Fig. 1; AAPA) except that does not teach prior to producing said first HDLC encoded data, receiving said first

5   HDLC encoded data from an PCM highway.

Mergard teaches a High-Level Data Link Controller (viz., HDLC controller), wherein Channels of HDLC controller can be coupled to a radio carrier station (i.e., Radio Carrier Station) is an PCM highway (See col. 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

10   made to have included said HDLC controller, as disclosed by Mergard, in said RCS, as disclosed by Pillan, as modified by Shimizu and AAPA, for the advantage of providing a broad range of communications applications (See Mergard, col. 1, lines 25-27).

Pillan, as modified by Shimizu, AAPA and Mergard, teaches prior to producing said first HDLC encoded data, receiving said first HDLC encoded data from said PCM highway.

15   ***Response to Arguments***

10.   Applicants' arguments filed on 2nd of January 2004 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to claims 1-20, "Koenig et al. does not disclose two processors communicating using parallel data highways. ... Accordingly, Koenig does not

20   disclose 'a second processor sending data using a single one of the data highways' as recited in claim 1, for example. ..." on the Response page 9, lines 8-17, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, Koenig suggests the above argued elements, such that DSP (Host) 22 of Fig. 4 (i.e., a second processor) sending data for Internet, video, or WAN applications (See col. 7, lines 65-67) using a V.35 high-speed serial port 64 in Fig. 4 (i.e., a single one of said data

highways, such that PCM highways 36, 38, 40, 42, 52, 54, 56, 58 and V.35 high-speed serial port 64 in

Fig. 4). Furthermore, it is noted that the features upon which applicants rely (i.e., two processors

communicating using parallel data highways) are not recited in the rejected claim(s). Although the claims

are interpreted in light of the specification, limitations from the specification are not read into the claims.

5   See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicants' argument on this point is not persuasive.

      In response to the Applicants' argument with respect to claims 21-23, "there is no motivation or

suggestion in Pillan to combine it with any of the other references as the claimed invention. Accordingly,

Pillan clearly teaches away from using a second HDLC encoding as in the present invention. Such an

10   encoding would clearly increase the data rate, which Pillan is clearly trying to avoid. ..." on the Response

page 9, line 18 through page 10, line 9, the Examiner respectfully disagrees.

First of all, it is noted that the features upon which applicants rely (i.e., dual encoding, such that a first

HDLC encoding and a second HDLC encoding, increases the data rate) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from the

15   specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed.

Cir. 1993).

Secondly, in contrary to the Applicants' statement, i.e., Pillan is clearly trying to avoid increasing the data

rate, the object of Pillan's invention is also increasing the data rate by way of reducing the data frame

using compression (See Summary of the Invention).

20   Thirdly, there is not any evidence in the specification, which could support the Applicants' assertion, such

that the claimed encoding would clearly increase the data rate. Further, the arguments of counsel cannot

take the place of evidence in the record. *In re Schulze,* 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA

1965). See M.P.E.P. 716.01(c).

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to claims 21-23, "Additionally, Shimizu

discloses essentially ... In the HDLC encoding, the data is encoded and then that encoded data including

all of the added information is then encoded in the same format. That is totally different than Shimizu."

on the Response page 10, lines 19-25, the Examiner respectfully disagrees.

5   First of all, it is noted that the features upon which applicants rely (i.e., encoded data including all of the

added information) are not recited in the rejected claim(s). Although the claims are interpreted in light of

the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988

F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Secondly, in contrary to the Applicants' assertion, the Applicants do not recite "In the HDLC encoding,

10   the data is encoded and then that encoded data is then encoded in the same format", but do recite "In the

HDLC encoding, the data is encoded and then that encoded data is then encoded in the second format"

(See Claim 21, lines 4-7).

Thirdly, the result of double HDLC encoding in the claimed invention contributes to allow for error

correction (See Application, page 7, lines 16-18), which is the same as the object of the Shimizu's

15   invention (See Shimizu, col. 1, lines 65+).

Thus, the Applicants' argument on this point is not persuasive.

Conclusion

11.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set

forth in 37 CFR 1.136(a).

20   A shortened statutory period for reply to this final action is set to expire THREE MONTHS from

the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing

date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX

MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally

5   be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark

H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application

10   Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

15

Christopher E. Lee
Examiner
Art Unit 2112

cel/ *signature*

signature
Glenn A. Auve
Primary Patent Examiner
Technology Center 2100